HA-2544
SPICE OPERATIONAL AMPLIFIER MACRO-MODEL

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Introduction

This application note describes the SPICE macro-model for the HA-2544, an op amp designed specifically for video applications. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the Spice net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model is designed to emulate a typical rather than a worst case part. Most AC and DC paramaters are simulated. Significant poles and zeros are included to give the most accurate AC and transient simulation with minimum complexity.

Model Description

Input Stage

DP and DN represent the differential input resistance. Input bias currents are created by I1 and offset current is modeled with FA. Source VIO represents the input offset voltage. C1 limits slew rate. No input parasitics due to package capacitance and lead inductance are included.

Gain Stage

G2, R2, CC, GOL, and RD simulate open loop gain. CC is the macro-model dominant pole capacitor.

Poles and Zeros

The HA-2544 macro-model utilizes six poles and one zero to simulate frequency response. RC networks create the poles and RL networks create the zero. Singularity frequencies are indicated on the schematic. Instructions for converting the model to have a simple two pole response are included in the netlist. This reduces simulation time at the expense of accurate frequency response.

Output Stage

EX1, D1 and D2 model output current limiting. IH and IL model the power supply currents. FIP and FIN vary the supply currents based on the op amp's output current. DL, DH, VH and VL provide voltage clamping on the output to simulate the typical output voltage swing. No output parasitics due to package capacitance and lead inductance are included.

Parameters Not Modeled

To maintain a simple macro-model not all op amp parameters are modeled. Most of the parameters not modeled are listed below:

- Temperature Effects
- Differential Voltage Restrictions
- Input Voltage and Current Noise
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Power Supply Range

Spice Listing

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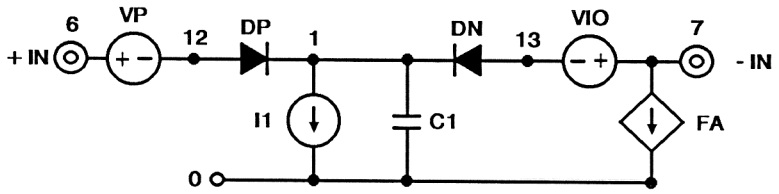
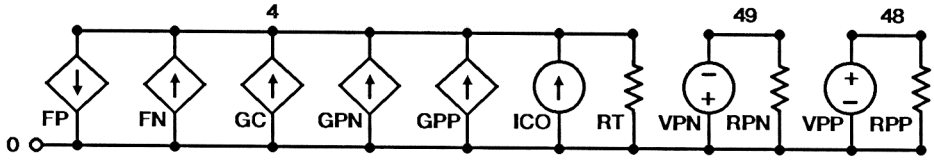
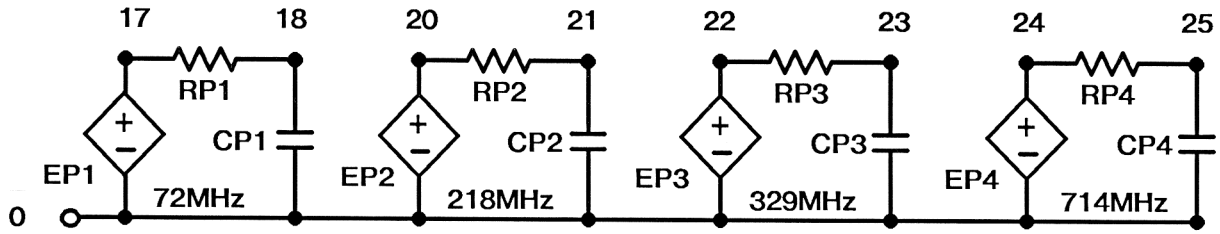
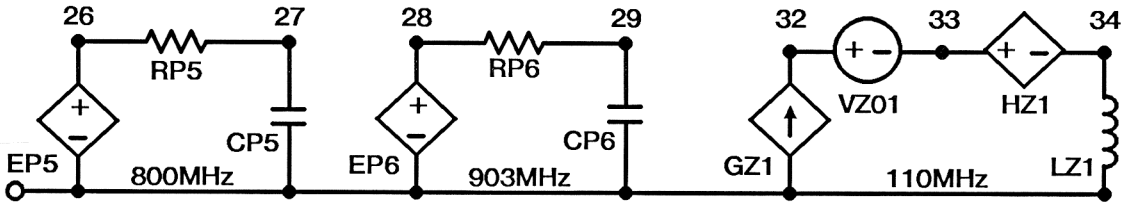
*
*HA-2544 MACRO MODEL
*REV: 4/19/91
*BY: D. L. YOUNGBLOOD
*
*PINOUT   +IN   -IN   VCC   VEE   VOUT
*
.SUBCKT   HA2544   6   7   9   10   8
.MODEL DP D      IS=1E-14          N=+1.384E+01
.MODEL DN D      IS=+9.7533E-15 N=+1.384E+01
.MODEL DV D      IS=+6.2773E-16 N=.1
.MODEL D1 D      IS=1E-14          N=1
.MODEL D2 D      IS=1E-14          N=+5.0E-01
*
*INPUT STAGE
*
VP 6 11 0
DP 11 1 DP
*
*THE VALUE OF SOURCE "VIO" REPRESENTS OFFSET
*VOLTAGE AND MAY BE CHANGED TO SIMULATE
*WORST CASE IF DESIRED
*
VIO 7 12 -2.7757E-04
*
DN 12 1 DN
FA 7 0 VIO +1.0636E-02
I1 1 0 +1.6994E-05
C1 1 0 +1.4933E-15      IC=-7.3159
FP 4 0 VP   +2.1354E+02
FN 0 4 VIO   +2.1894E+02
GPP 0 4 9 13 +4.9937E-07
GPN 0 4 14 10 +2.6098E-07
RT 4 0 1
VPP 13 0 +1.5E+01
RPP 13 0 1K
VPN 0 14 +1.5E+01
RPN 0 14 1K
GC 0 4 1 0 +7.1701E-11
ICO 0 4 5.2461E-10
*
*GENERAL POLES
*
EP1 17 0 4 0 1
RP1 17 18 +2.1953E+01
CP1 18 0 1.0E-10
EP2 20 0 18 0 1
RP2 20 21 +7.2843
CP2 21 0 1.0E-10
EP3 22 0 21 0 1
RP3 22 23 +4.8433
CP3 23 0 1.0E-10
EP4 24 0 23 0 1
RP4 24 25 +2.2283
CP4 25 0 1.0E-10
EP5 26 0 25 0 1
RP5 26 27 +1.9908
CP5 27 0 1.0E-10
EP6 28 0 27 0 1
RP6 28 29 +1.6526
CP6 29 0 1.0E-10
*
*GENERAL ZERO
*
GZ1 0 32 29 0 +1.4448E-03
VZ01 32 33 0.0
HZ3 33 34 VZ01   +6.9216E+02
LZ1 34 0 1.0E-6
*
*GAIN/OUTPUT STAGE
*
*FOR A LEVEL 1 MODEL, CHANGE NODE 32 ON
*SOURCE "G2" TO 4, ADD A CAPACITOR FROM
*NODE 4 TO NODE 0 OF THE VALUE 1.69E-9, AND
*COMMENT OUT ALL GENERAL POLES AND ZEROS
*
G2 0 2 32 0 1
*
R2 2 0 +1.7546E+05
CC 2 3 +2.2E-11
GOL 3 0 2 0 +7.8868E-02
RD 3 0 +9.1695E+01
DH 3 5 DV
DL 40 3 DV
VH 9 5 3.7914
VL 40 10 1.9075
IH 9 0 +1.0591E-02
IL 0 10 +1.0608E-02
D1 3 43 D1
D2 43 3 D2
EX1 43 0 POLY   2   3   0   3   8   0   1   -1.2895E-01
RO 44 8 +2.7421E+01
VIS 3 44 0
FI 0 45 VIS   1
DIP 45 46 DV
DIN 48 47 DV
VIP 46 48 0
VIN 47 45 0
RI 48 0 1
FIP 9 0 VIP   1
FIN 0 10 VIN   1
.ENDS HA2544
```

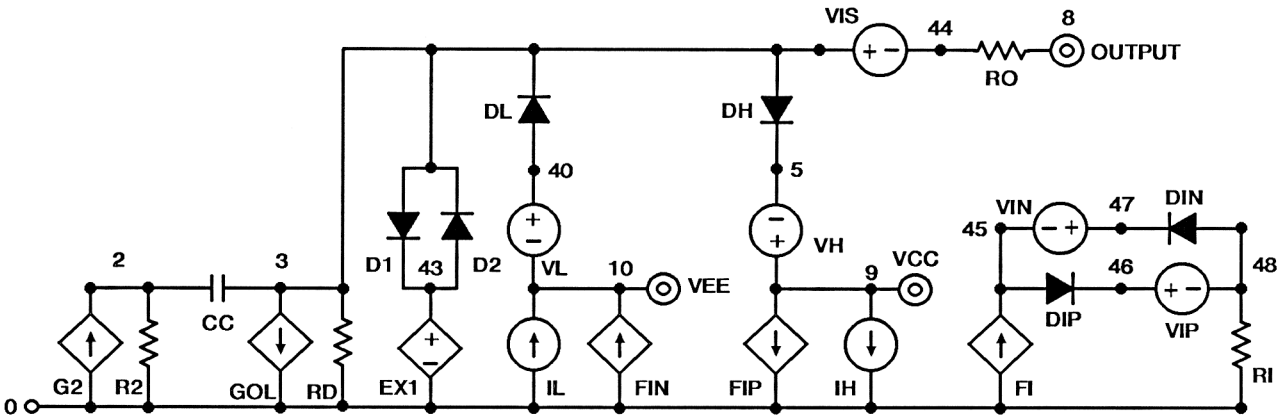
Macro-Model Schematic





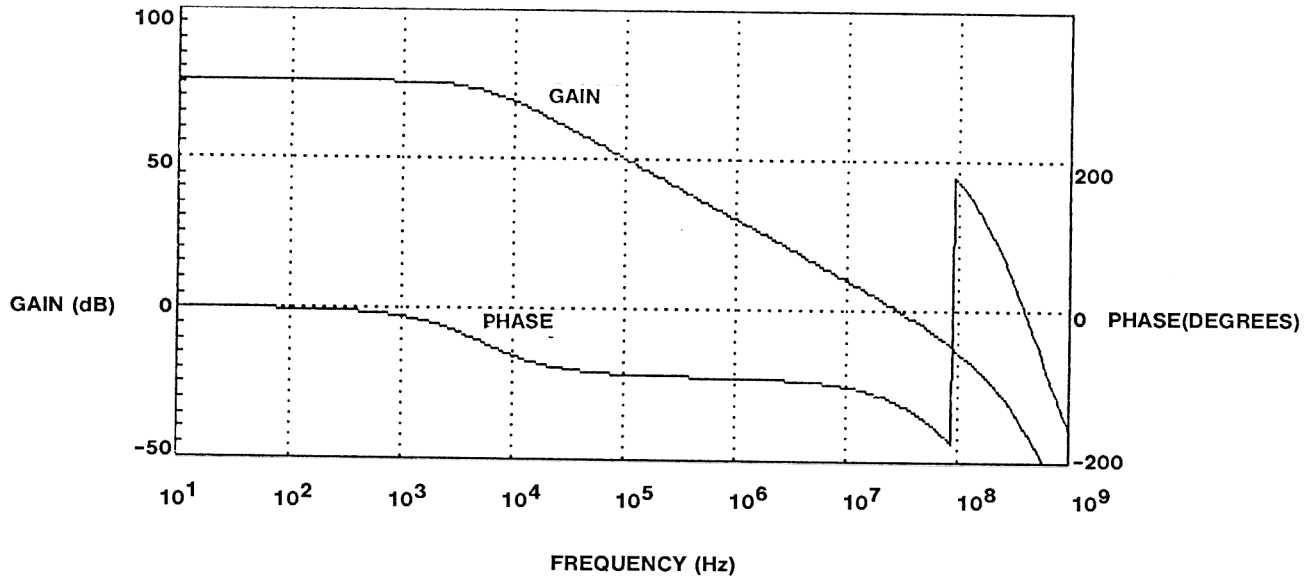




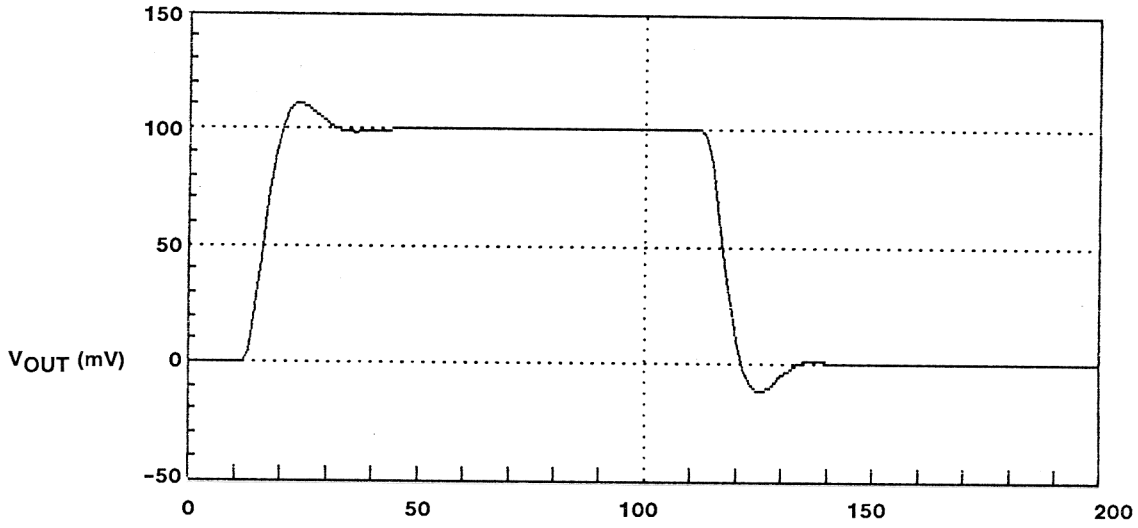


Model Performance Conditions V_{SUPPLY} = ±15 V, A_{VCL} = +1, Unless Otherwise Specified

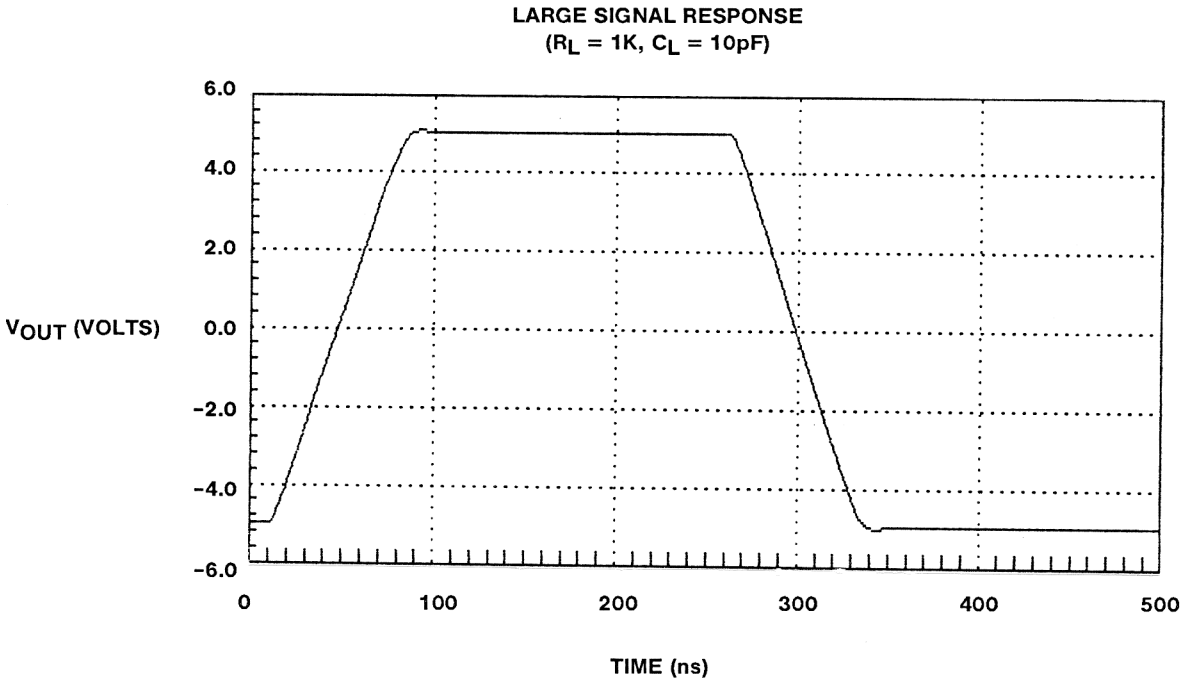
OPEN LOOP GAIN AND PHASE vs FREQUENCY
(R_L = 1K, C_L = 10pF)



SMALL SIGNAL RESPONSE
(R_L = 1K, C_L = 10pF)



Model Performance (Continued) Conditions: V_{SUPPLY} = ±15V, A_{VCL} = +1, Unless Otherwise Specified



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